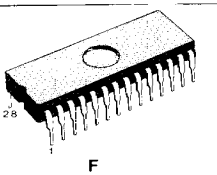
64K (8K x 8) UV ERASABLE PROM

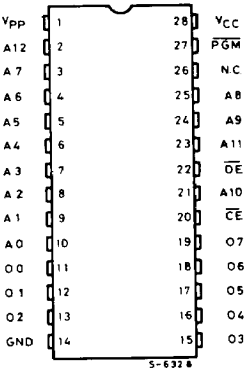
- FAST ACCESS TIME:
  200ns MAX M2764-2F1
  250ns MAX M2764F1/-25F1/F6
  300ns MAX M2764-3F1/-30F1
  450ns MAX M2764-4F1/-45F1/-4F6
- SINGLE +5V POWER SUPPLY
- LOW STANDBY CURRENT 40mA MAX
- INPUTS AND OUTPUTS TTL COMPATIBLE DURING READ AND PROGRAM
- COMPLETELY STATIC



F
Ceramic Package

ORDERING NUMBERS: M2764HF1
M2764H-2F1
M2764H-3F1
M2764H-4F1
M2764H-25F1
M2764H-30F1
M2764H-45F1
M2764HF6
M2764H-4F6

PIN CONNECTIONS



PIN NAMES

A0-A12	ADDRESS INPUT
$\overline{CE}$	CHIP ENABLE INPUT
$\overline{OE}$	OUTPUT ENABLE INPUT
$\overline{PGM}$	PROGRAM
N.C.	NO CONNECTION
O0-O7	DATA INPUT/OUTPUT

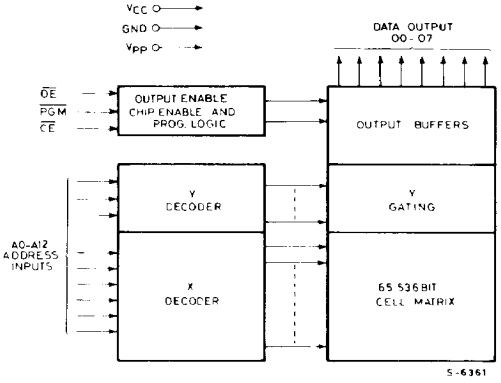
DESCRIPTION

The M2764 is a 65,536-bits ultraviolet erasable and electrically programmable read-only memory (EPROM). It is organized as 8,192 words by 8 bits and manufactured using SGS' N-channel Si-Gate MOS process.

The M2764 with its single +5V power supply and with an access time of 200ns, is ideal for use with the high performance +5V microprocessor such as Z8®, Z80® and Z8000™. The M2764 has an important feature which is the separate the output control, Ouptut Enable ($\overline{OE}$) from the Chip Enable control ($\overline{CE}$). The $\overline{OE}$ control eliminates bus contention in multiple bus microprocessor systems.

The M2764 also features a standby mode which reduces the power dissipation without increasing access time. The active current is 100mA while the maximum standby current is only 40mA, a 60% saving. The standby mode is achieved by applying a TTL-high signal to the $\overline{CE}$ input.
The M2764 is available in a 28-lead dual in-line ceramic package glass lens. (frit-seal)

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_I	All Input or Output voltages with respect to ground	+ 7 to −0.6	V
V_{PP}	Supply voltage with respect to ground during program	+22 to −0.6	V
T_{amb}	Ambient temperature under bias /F1/-2F1/-3F1/-4F1/ /-25F1/-30F1/-45F1 /F6-4F6	−10 to + 80	°C
T_{stg}	Storage temperature range	−65 to + 125	°C

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating o and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specificat is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

OPERATING MODES

MODE \ PINS	$\overline{CE}$ (20)	$\overline{OE}$ (22)	$\overline{PGM}$ (27)	V_{PP} (1)	V_{CC} (28)	OUTPUT
READ	V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	D_{OUT}
STANDBY	V_{IH}	X	X	V_{CC}	V_{CC}	HIGH Z
PROGRAM	V_{IL}	X	V_{IL}	V_{PP}	V_{CC}	D_{IN}
PROGRAM VERIFY	V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	D_{OUT}
PROGRAM INHIBIT	V_{IH}	X	X	V_{PP}	V_{CC}	HIGH Z

X = Don't care

READ OPERATION
DC AND AC CONDITIONS

	F1/ – 2F1 – 3F1/ – 4F1	– 25F1/ – 30F1/ – 45F1	F6/ – 4F6
Operating Temperature Range	0 to 70°C	0 to 70°C	– 40 to 85°C
V_{CC} Power Supply (1,2)	5V ±5%	5V ±10%	5V ±5%
V_{PP} Voltage (2)	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$	$V_{PP} = V_{CC}$

DC AND OPERATING CHARACTERISTICS

Symbol	Parameter	Test Conditions	Values			Unit
			Min.	Typ.(3)	Max.	
I_{LI}	Input Load Current	$V_{IN} = 5.5V$			10	μA
I_{LO}	Output Leakage Current	$V_{OUT} = 5.5V$			10	μA
I_{PP1}(2)	V_{PP} Current Read	$V_{PP} = 5.5V$		2	5	mA
I_{CC1}(2)	V_{CC} Current Standby	$\overline{CE} = V_{IN}$			40	mA
I_{CC2}(2)	V_{CC} Current Active	$\overline{CE} = \overline{OE} = V_{IL}$		50	100	mA
V_{IL}	Input Low Voltage		– 0.1		+ 0.8	V
V_{IH}	Input High Voltage		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage	$I_{OL} = 2.1$ mA			0.45	V
V_{OH}	Output High Voltage	$I_{OH} = -400$ μA	2.4			V

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions	2764-2		2764 2764-25		2764-3 2764-30		2764-4 2764-45		Unit
			Min	Max	Min	Max	Min	Max	Min	Max	
t_{ACC}	Address to Output Delay	$\overline{CE} = \overline{OE} = V_{IL}$		200		250		300		450	ns
t_{CE}	$\overline{CE}$ to Output Delay	$\overline{OE} = V_{IL}$		200		250		300		450	ns
t_{OE}	$\overline{OE}$ to Output Delay	$\overline{CE} = V_{IL}$		75		100		120		150	ns
t_{DF}(4)	$\overline{OE}$ High to Output Float	$\overline{CE} = V_{IL}$	0	60	0	85	0	105	0	130	ns
t_{OH}	Output Hold from Address $\overline{CE}$ or $\overline{OE}$ Whichever Occurred First	$\overline{CE} = \overline{OE} = V_{IL}$	0		0		0		0		ns

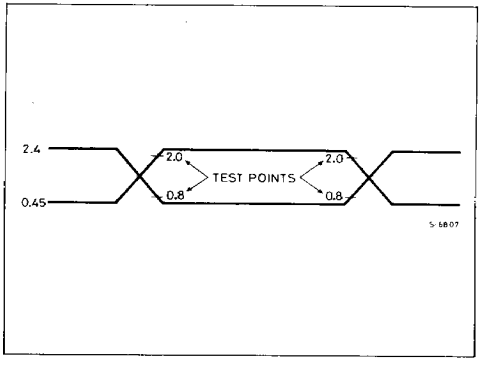
CAPACITANCE(5) ($T_{amb} = 25°C$, f = 1 MHz)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
C_{IN}	Input Capacitance	$V_{IN} = 0V$		4	6	pF
C_{OUT}	Output Capacitance	$V_{OUT} = 0V$		8	12	pF

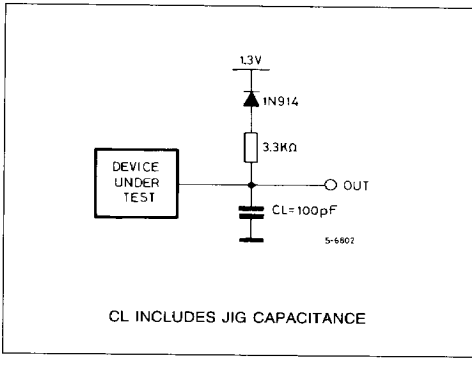
Notes:
1. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.
2. V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.
3. Typical values are for $T_{amb} = 25°C$ and nominal supply voltages.
4. This parameter is only sampled and not 100% tested. Output Float is defined as the point where data is no longer driven-see timing diagram.
5. This parameter is only sampled and not 100% tested.

AC TEST CONDITIONS
Output Load: 100pF + 1TTL Gate
Input Rise and Fall Times: $\leq$ = 20ns
Input Pulse Levels: 0.45 to 2.4V
Timing Measurement Reference Levels: Inputs 0.8 and 2V
Outputs 0.8 and 2V

AC TESTING INPUT/OUTPUT WAVEFORM

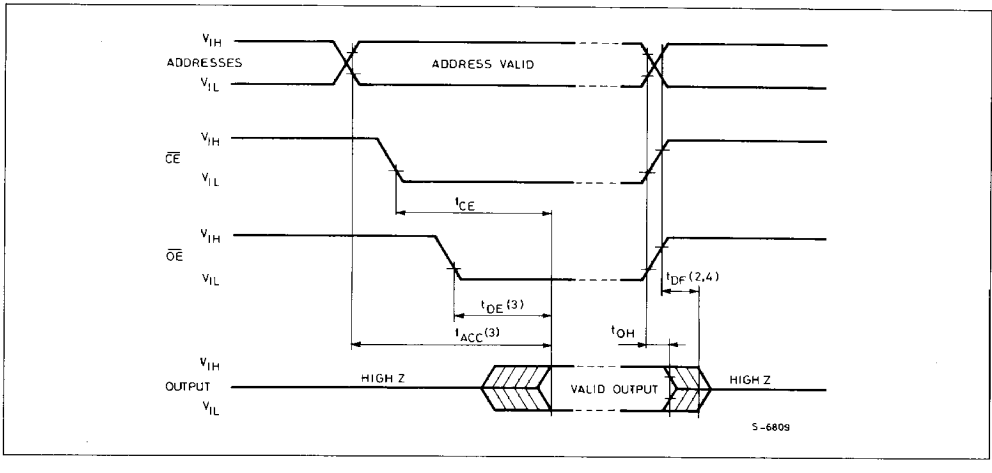


AC TESTING LOAD CIRCUIT



CL INCLUDES JIG CAPACITANCE

AC WAVEFORMS



Notes:
1. Typical values are for T_{amb} = 25°C and nominal supply voltage.
2. This parameter is only sampled and not 100% tested.
3. $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge $\overline{CE}$ without impact on t_{ACC}.
4. t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$ whichever occurs first.

READ MODE

The M2764 has two control functions, both of which must be logically satisfied in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data to the output pins, independent of device selection. Assuming that addresses are stable, address access time (t_{ACC}) is equal to delay from $\overline{CE}$ to output (t_{CE}). Data is available at the outputs after the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least t_{ACC}-t_{OE}.

STANDBY MODE

The M2764 has a standby mode which reduces the active power current by 60%, form 100mA to 40 mA. The M2764 is placed in the standby mode by applying a TTL high signal to the $\overline{CE}$ input. When in the standby mode, the outputs are in a high impedance state, independent of the $\overline{OE}$ input.

OUTPUT OR-TIEING

Because M2764's are usually used in larger memory arrays, the product features a 2 line control function which accommodates the use of multiple memory connection. The two line control function allows:

a) the lowest possible memory power dissipation
b) complete assurance that output bus contention will not occur.

To most efficiently use these two control lines, it is recommended that $\overline{CE}$ be decoded and used as the primary device selecting function, while $\overline{OE}$ should be made a common connection to all devices in the array and connected to the $\overline{READ}$ line from the system control bus. This assures that all deselected memory devices are in their low power standby mode and that the output pins are only active when data is desired from a particular memory device.

PROGRAMMING

Caution: exceeding 22V on pin (V_{PP}) will damage the M2764.

When delivered, and after each erasure, all bits of the M2764 are in the "1" state. Data is introduced by selectively programming "0s" into the desired bit locations. Although only "0s" will be programmed, both "1s" and "0s" can be present in the data word. The only way to change a "0" to a "1" is by ultraviolet light erasure. The M2764 is in the programming mode when V_{PP} input is at 21V and $\overline{CE}$ is at TTL low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

For programming, $\overline{CE}$ should be kept TTL-low at all times while V_{PP} is kept at 21V. When the addresses are stable, a 50ms, active-low, TTL program pulse is applied to the $\overline{PGM}$ input. A program pulse must be applied at each address location to be programmed. You can program any location at any time either individually, sequentially, or at random. The program pulse has a maximum width of 55ms.

FAST PROGRAMMING ALGORITHM

Fast Programming Algorithm rapidly programs M2764 EPROMs using an efficient and reliable method particularly suited to the production programming enviroment. Typical programming times for individual devices are on the order of 1.25 minutes. Programming reliability is also ensured as the incremental program margin of each bytes is continually monitored to determine when it has been successfully programmed. A flowchart of the Fast Programming Algorithm is shown in last page.

The Fast Programming Algorithm utilizes two different pulse types: initial and overprogram.

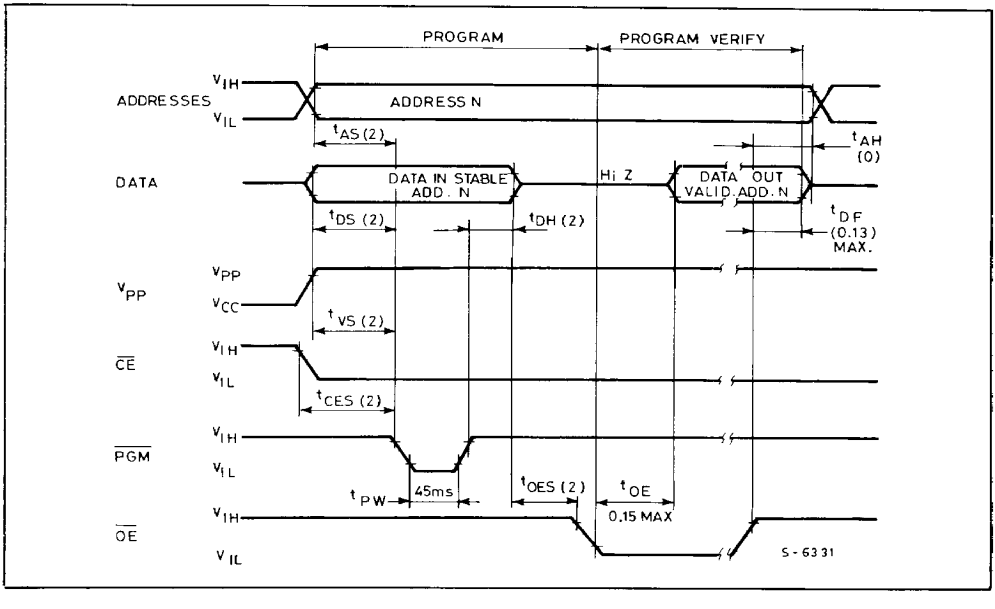
The duration of the initial $\overline{CE}$ pulse (s) is one millisecond, which will then be followed by a longer overprogram pulse of length 4X msec (X is an iteration counter and is equal to the number of the initial one millisecond pulses applied to a particular M2764 location), before a correct verify occurs. Up to 15 one-millisecond pulses per byte are provided for before the over program pulse is applied. The entire sequence of program pulses and byte verifications is performed at $V_{CC} = 6.0V$ and $V_{PP} = 21.0V$. When the Fast Programming cycle has been completed, all bytes should be compared to the original data with $V_{CC} = V_{PP} = 5.0V$.

PROGRAM INHIBIT
Programming of multiple M2764s in parallel with different data is also easily accomplished. Except for $\overline{CE}$ (or $\overline{PGM}$), all like inputs (including $\overline{OE}$) of the parallel M2764s may be common. A TTL low pulse applied to a M2764 $\overline{CE}$ and $\overline{PGM}$ input, with V_{PP} at 21V will program that M2764. A high level $\overline{CE}$ input inhibits the other M2764s from being programmed.

PROGRAM VERIFY
A verify should be performed on the programmed bits to determine that they were correctly programmed. The verify is accomplished with $\overline{CE}$ and $\overline{OE}$ at V_{IL}. However, $\overline{PGM}$ is at V_{IH}.

ERASURE OPERATION
The erasure characteristic of the M2764 are such that erasure begins when the cells are exposed to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å range. Data shows that constant exposure to room level fluorescent lighting could erase a typical M2764 in approximately 3 years, while it would take approximately 1 week to cause erasure when expose to the direct sunlight. If the M2764 is to be exposed to these type of lighting conditions for extended periods of time, it is suggested that opaque labels to put over the M2764 window to prevent unintentional erasure. The recommended erasure procedure for the M2764 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e. UV intensity x exposure time) for erasure should be a minimum of 15 W-sec/cm^2. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with 12000 μW/cm^2 power rating. The M2764 should be placed within 2.5 cm of the lamp tubes during erasure. Some lamps have a filter on their tubes which should be removed before erasure.

PROGRAMMING WAVEFORMS



PROGRAMMING OPERATION (1)(T_{amb} = 25°C ±5°C, V_{CC}(2) = 5V ±5%, V_{PP}(2,3) = 21V ±0.5V)

DC AND OPERATING CHARACTERISTIC:

Symbol	Parameter	Conditions	Values			Unit
			Min.	Typ.	Max.	
I_{LI}	Input Current (All Inputs)	$V_{IN} = V_{IL}$ or V_{IH}			10	µA
V_{IL}	Input Low Level		−0.1		0.8	V
V_{IH}	Input High Level		2.0		V_{CC} + 1	V
V_{OL}	Output Low Voltage During Verify	I_{OL} = 2.1 mA			0.45	V
V_{OH}	Output High Voltage During Verify	I_{OH} = −400 µA	2.4			V
I_{CC2}	V_{CC} Supply Current (Active)				100	mA
I_{PP}	V_{PP} Supply Current	$\overline{CE} = \overline{PGM} = V_{IL}$			30	mA

AC CHARACTERISTICS

Symbol	Parameter	Test Conditions (See note 2)	Values			Unit
			Min.	Typ.	Max.	
t_{AS}	Address Setup Time		2			µs
t_{OES}	$\overline{OE}$ Setup Time		2			µs
t_{DS}	Data Setup Time		2			µs
t_{AH}	Address Hold Time		0			µs
t_{DH}	Data Hold Time		2			µs
t_{DFP}(6)	Output Enable Output Float Delay		0		130	ns
t_{VPS}	V_{PP} Setup Time		2			µs
t_{VCS}	V_{CC} Setup Time		2			µs
t_{PW}	Initial Program Pulse Width	(see Note 4)	0.95	1.0	1.05	ms
t_{OPW}	$\overline{CE}$ Overprogram Pulse Width	(see note 5)	3.8		63	ms
t_{OE}	Data Valid from $\overline{OE}$				150	ns

Notes:
1. SGS guarantees the product only if it is programmed to specifications described herein.
2. V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}. The M2764 must not be inserted into or removed from a board with V_{PP} at 21 ±0.5V or damage may occur to the device.
3. The maximum allowable voltage which may be applied to the V_{PP} pin during progamming is +22V. Care must be taken when switching the V_{PP} supply to prevent overshoot exceeding this 22V maximum specification.
4. Initial Program Pulse width tolerance is 1msec ±5%.
5. The length of the overprogram pulse may vary from 3.8 msec to 63 msec as a function of the iteration counter value X.
6. This parameter is only sampled and is not 100% tested.
   Output Float is defined as the point where data is no longer driven (see timing diagram).

FAST PROGRAMMING FLOWCHART