DUAL MASTER-SLAVE JK FLIP-FLOP

FCJ121

DEVELOPMENT SAMPLE DATA

The FCJ121 is a monolithic integrated circuit containing two direct-coupled JK flip-flops. With the exception of the SET terminal which is common to both flip-flops the circuits operate independently of each other.

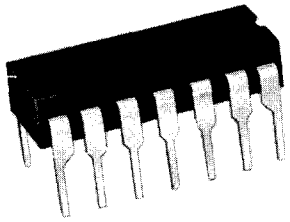
QUICK REFERENCE DATA		
Supply voltage (nominal)	+6.0	V
Operating temperature range	0 to +75	^{o}C
Fan-out capability to FC gates at 25^{o}C (min.)	8	
Clock rate (full temperature range)	0 to 4.0	MHz
Total power dissipation (typ.) (50% duty cycle, T_{amb} = 25^{o}C) each flip-flop	50	mW

Unless otherwise stated data is applicable to individual flip-flops

OUTLINE AND DIMENSIONS

14 lead dual-in-line package

For details see General Explanatory Notes



LOGIC FUNCTION

Operation of the FCJ121 depends on voltage levels only i.e. rise and fall times of all input signals are immaterial. The information at the J and K inputs enters the master when the trigger T is 'High'. Subsequently when the trigger input is 'Low', the information is transferred from master to slave and it appears at the outputs.

The direct SET input S which overrides any other input is active at the 'Low' level influencing both master and slave. One of the flip-flops has 2 J inputs (AND function) which simplifies counter systems. Inputs not needed may be left floating, the result is the same as if a 'High' signal were applied.

DESIGN DATA

Over the full temperature range 0 to 75°C

		Min.	Nom.	Max.	
Supply					
Supply voltage		5.7	6.0	6.3	V
Current consumption from supply					
50% duty cycle, V_{supply} = 6.0V		-	16.8	-	mA
T 'Low', V_{supply} = 6.0V		-	17.7	-	mA
Input					
Voltage for 'High' input state					
J, K and T inputs	S.N.I. = 0	2.6	-	6.3	V
	S.N.I. = 1.3V	3.9	-	6.3	V
SET input	S.N.I. = 0	1.9	-	6.3	V
	S.N.I. = 2.0V	3.9	-	6.3	V
Current for 'High' input state					
J or K inputs		-	-	25	μA
T inputs		-	-	75	μA
SET input		-	-	100	μA
Voltage for 'Low' input state					
J or K inputs	S.N.I. = 0	-	-	1.1	V
	S.N.I. = 0.7V	-	-	0.4	V
SET and T inputs	S.N.I. = 0	-	-	0.7	V
	S.N.I. = 0.3V	-	-	0.4	V
Current for 'Low' input state (full temperature range, see curve on page 8 for other temperatures)					
J or K inputs		-	-	1.6	mA
T inputs		-	-	4.5	mA
SET input		-	-	6.6	mA
Output					
Voltage for 'High' output state		3.9	-	6.3	V
Voltage for 'Low' output state		-	-	0.4	V
Current capability at 'Low' output state (T_{amb} = 75°C, see curve on page 8 for other temperatures)		-	-	12.4	mA

DESIGN DATA (cont'd)

Output (cont'd)

D.C. Fan-out	Max.
1. Uniform system temperature and voltage	
FC gates	8
J or K inputs	10
T inputs	3
SET inputs	2
2. Uniform system temperature, adjacent circuits at extremes of supply voltage	
FC gates	6
J or K inputs	8
T inputs	3
SET inputs	2
3. Adjacent circuits at extremes of temperature and supply voltage	
FC gates	6
J or K inputs	7
T inputs	2
SET inputs	1

Truth tables

1. Trigger action via terminal T. The information at J and K is transferred to the master when T becomes 'High'. The outputs assume the levels indicated after a subsequent transition of T to 'Low'. The SET input S should be 'High' or floating.

Conditions before transition		Output after transition	
J	K	Q1	Q2
H	H	Reversed	
L	H	L	H
H	L	H	L
L	L	No change	

J11	J12	J
H	H	H
L	H	L
H	L	L
L	L	L

For the flip-flop with two J inputs the second table gives the J signal to be used in the first table.

DESIGN DATA (cont'd)

Truth tables (cont'd)

2. Clear action via S (both flip-flops)

The S input influences the outputs of both flip-flops irrespective of the signals at any other input including the T input.

S	Q11	Q12	Q21	Q22
L	L	H	L	H
H	No change		No change	

H = 'High' state normally corresponding to a voltage level between 3.9 and 6.3V.

L = 'Low' state normally corresponding to a voltage level between 0 and 0.4V.

PERFORMANCE

		Min.	Nom.	Max.	
Signal noise immunity					
J or K inputs	'Low' state	0.7	-	-	V
	'High' state	1.3	-	-	V
T inputs	'Low' state	0.3	-	-	V
	'High' state	1.3	-	-	V
S input	'Low' state	0.3	-	-	V
	'High' state	2.0	-	-	V
Clock rate		-	-	4.0	MHz

CHARACTERISTICS

Supply voltage = +6.0V, $T_{amb} = 25^{o}C$

		Min.	Typ.	Max.	
V_{TH} 'Low'	Input threshold voltage for 'Low' input state (V_{out} = 4.2V, I_{out} = 0)				
	SET input (see note 1)	1.0	-	-	V
	J or K inputs (see note 2)	1.4	-	-	V
	T input (see note 3)	1.0	-	-	V
V_{TH} 'High'	Input threshold voltage for 'High' input state (V_{out} = 0.4V, I_{out} = 17.7mA)				
	SET input (see note 4)	-	-	1.8	V
	J or K inputs (see note 5)	-	-	2.3	V
	T input (see note 6)	-	-	2.3	V
V_{out} 'Low'	Output voltage for 'Low' output state ($V_{in(SET)}$ = 1.8V, I_{out} = 17.7mA)	-	-	0.4	V

CHARACTERISTICS (cont'd)

		Min.	Typ.	Max.	
I_{in} 'High'	Input current for 'High' input state (V_{in} = 6.0V, all other inputs = 0V)				
	J or K inputs	-	-	1.0	μA
	T inputs	-	-	3.0	μA
	SET input	-	-	4.0	μA
I_{in} 'Low'	Input current for 'Low' input state (V_{in} = 0.4V)				
	J or K inputs	-	-	1.4	mA
	T inputs	-	-	4.0	mA
	SET inputs	-	-	5.9	mA

NOTES

1. The SET input must be in the 'Low' state for at least 120ns.
2. The output will not change state on the application of a trigger pulse if $V_J < V_{TH}$ 'Low'.
3. Information in the master will be transferred to the slave if $V_T < V_{TH}$ 'Low' for > 120ns.
4. The SET input is inactive if $V_S > V_{TH}$ 'High'.
5. The output will change state on the application of a trigger pulse if $V_J > V_{TH}$ 'High'.
6. The master will be set by JK information if $V_T > V_{TH}$ 'High' for 60ns.

	Min.	Typ.	Max.	
Dynamic				
Repetition frequency	-	-	4.0	MHz

RATINGS

Limiting values of operation according to the absolute maximum system.

Electrical

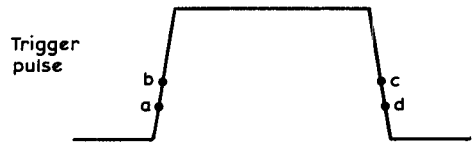
Maximum positive supply voltage (pin 7)	8.0	V
Maximum positive output voltage (pins 1, 2, 11, 12)	8.0	V
Maximum negative output voltage (pins 1, 2, 11, 12)	0	V
Maximum positive input voltage (pins 3, 4, 5, 6, 8, 9, 10, 13)	8.0	V
Maximum negative input current	20	mA

RATINGS (cont'd)

Temperature

T_{stg} range	−55 to +125	°C
T_{amb} range operating	0 to +75	°C

MASTER-SLAVE OPERATION

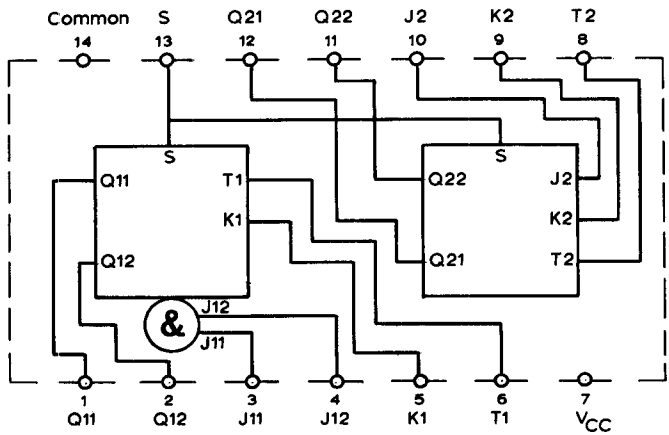


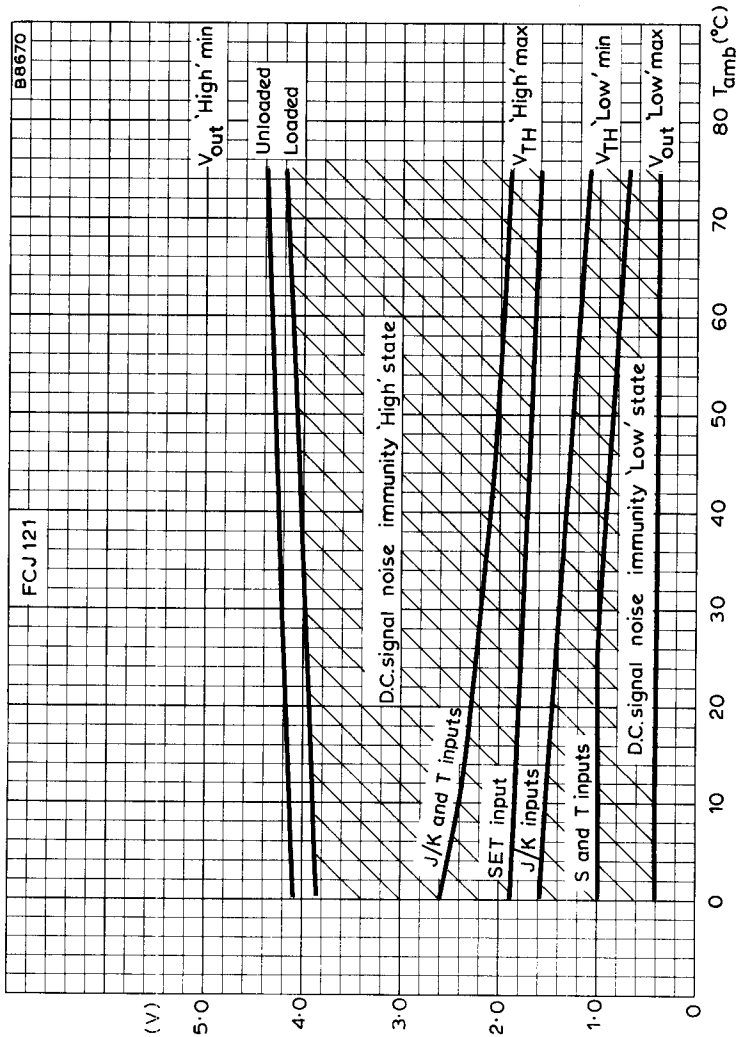
(a) Slave isolated from master
(b) JK information enters master
(c) Master disconnected from JK inputs
(d) Information transferred from master to slave

PINNING

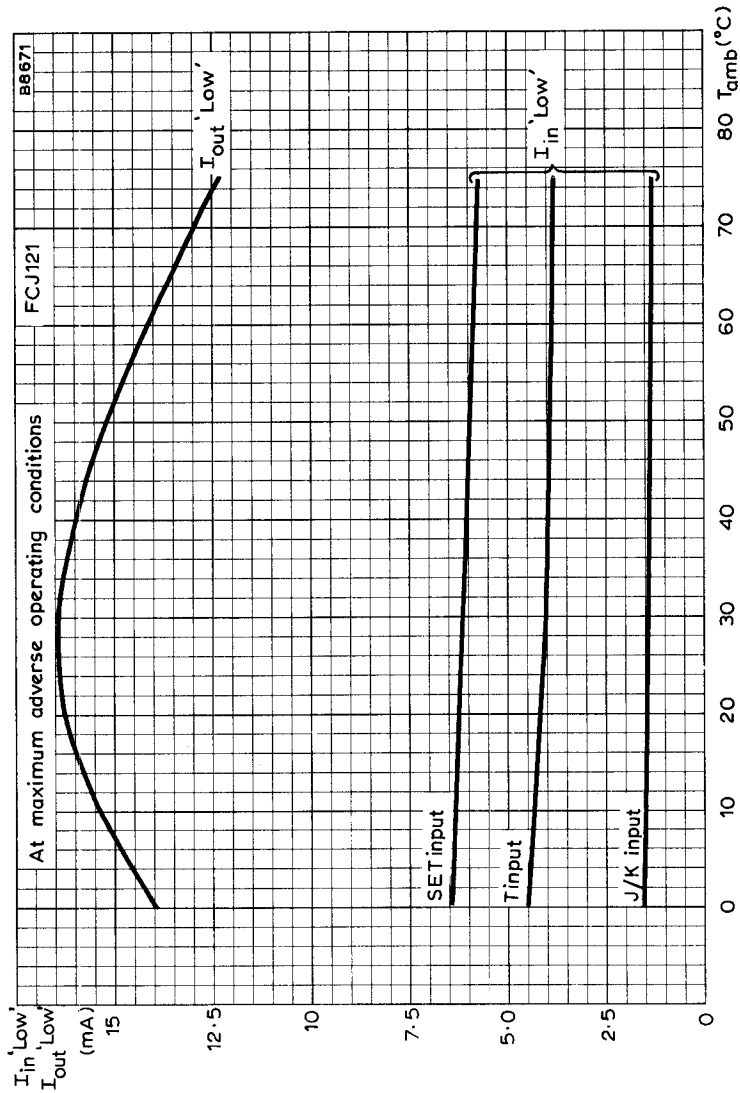
1.	Output Q11	8.	Input T2
2.	Output Q12	9.	Input K2
3.	Input J11	10.	Input J2
4.	Input J12	11.	Output Q22
5.	Input K1	12.	Output Q21
6.	Input T1	13.	Input S
7.	Positive supply	14.	Common and earth

LOGIC DIAGRAM





DESIGN CURVE
VARIATION OF D.C. LEVELS WITH TEMPERATURE



DESIGN CURVE
VARIATION OF OUTPUT AND INPUT CURRENTS
WITH AMBIENT TEMPERATURE